

ISSUE CLASSIFICATION	
Subclass	Class

**PATENT NUMBER**

**U.S. UTILITY Patent Application**

O.I.P.E.	<i>CH</i>	PATENT DATE
SCANNED <i>BK</i> (3)	Q.A. <i>Cx</i>	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/652003		711	154	2185 2186	W. Choi <u>JK</u>

## APPUCANTS

Graham Kirsch

title

Method and apparatus for connecting a massively parallel processor array to a memory array in a bit serial manner

PTO-2040  
12/89

## **ISSUING CLASSIFICATION**

Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
	(Assistant Examiner) _____ (Date)				
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____				ISSUE FEE	
	(Primary Examiner) _____ (Date)			Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				ISSUE BATCH NUMBER	
	(Legal Instruments Examiner) _____ (Date)				

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